Amendments to the Specification:

The paragraph beginning on page 3, line 15, has been amended as shown:

In a preferred embodiment, the aspects of the present invention are provided in the context of an embedded system environment employing an adaptive computing engine in accordance with the description in co-pending U.S. Patent application, serial no. ~~____~~ 09/815,122, entitled "Adaptive Integrated Circuitry with Heterogeneous and Reconfigurable Matrices of Diverse and Adaptive Computational Units Having Fixed, Application-Specific Computational Elements", assigned to the assignee of the present invention and incorporated by reference in its entirety herein. Portions of that description are reproduced hereinbelow for clarity of presentation of the aspects of the present invention.

The paragraph starting on page 5, line 15, has been amended as shown:

The various matrices 150 are reconfigurable and heterogeneous, namely, in general, and depending upon the desired configuration: reconfigurable matrix 150A is generally different from reconfigurable matrices 150B through 150N; reconfigurable matrix 150B is generally different from reconfigurable matrices 150A and 150C through 150N; reconfigurable matrix 150C is generally different from reconfigurable matrices 150A, 150B and 150D through 150N, and so on. The various reconfigurable matrices 150 each generally contain a different or varied mix of computation units, which in turn generally contain a different or varied mix of fixed, application specific computational elements, which may be connected, configured and reconfigured in various ways to perform varied functions, through the interconnection networks. In addition to varied internal configurations and reconfigurations, the various matrices 150 may be connected, configured and reconfigured at a higher level, with respect to each of the other

matrices 150, through the matrix interconnection network (MIN) 110. A more detailed discussion of the MIN is presented in co-pending U.S. Patent application, serial no. 09/898,350 ~~(Docket no. 2098P/QST-015 US)~~, entitled *Method and System for an Interconnection Network to Support Communications among a Plurality of Heterogeneous Processing Elements*, assigned to the assignee of the present invention, and incorporated herein by reference in its entirety.